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EXAMINER	
WANG, JIN CHENG	

ART UNIT	PAPER NUMBER
2628	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/858,354	MCCABE, DANIEL H.	
	Examiner	Art Unit	
	Jin-Cheng Wang	2628	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 April 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3-11,22,24-25 and 30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *30* is/are allowed.

6)☒ Claim(s) *1,3-11,22,24 and 25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendments

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission on 4/7/2006 has been entered. Claim 22 has been amended. Claims 2, 12-21, 23, and 26-29 have been canceled. Claim 30 has been newly added. Claims 1, 3-11, 22, 24-25 and 30 are pending in the present application.

Reasons for Allowance

1. The following is an examiner's statement of reasons for allowance of the base claim 30 in the amendment of 4/7/2006: Nothing in the prior art anticipates or suggests, "*the last sequential logic circuit configured to receive polygonal subportions, disregard any polygonal subportions thereof that are outside of the graphics primitive, and subdivide a remaining polygonal subportion into further equal polygonal subportions and output those further polygonal subportions*" in a system for identifying pixels inside a graphics primitive of a raster image, the system comprising: a memory for storing a raster image; and a graphics engine coupled to the memory and comprising a pipeline structure including: a sequential logic block comprising a plurality of identical sequential logic circuits coupled in series and including a first sequential logic circuit and a last sequential logic circuit, the first sequential logic circuit configured to receive a polygonal portion of the raster image from the memory and to either disregard the

polygonal portion if the polygonal portion is outside the graphic primitive or, if the polygonal portion is at least partly inside the graphics primitive, to subdivide the polygonal portion into equal polygonal subportions and output the polygonal subportions, and *the last sequential logic circuit configured to receive polygonal subportions, disregard any polygonal subportions thereof that are outside of the graphics primitive, and subdivide a remaining polygonal subportion into further equal polygonal subportions and output those further polygonal subportions;* and a parallel logic block comprising a plurality of identical parallel logic circuits including a first parallel logic circuit configured to receive the further polygonal subportions output from the last sequential logic circuit, disregard any further polygonal subportions thereof that are outside of the graphics primitive, and subdivide a remaining further polygonal subportion into still further equal polygonal subportions and output those still further polygonal subportions to two next parallel logic circuits operating in parallel.

Response to Arguments

Applicant's arguments filed April 7, 2006 have been fully considered but are moot in view of the ground(s) of rejection based on Duluk et al. U.S. Pat. No. RE38,078 (hereinafter Duluk) in view of Bowen et al. U.S. Patent No. 6,329,996 (hereinafter Bowen).

The base claim 1 set forth the claim limitation "each of the sequential logic circuits and each of the parallel logic circuits configured to receive a *different polygonal portion* of the raster image".

In applicant's disclosure related to this claim limitation in Fig. 11 and the corresponding specification, for example, Page 23-24, "sequential logic circuit 1102 may sequentially perform

subdivision processing and edge function... provided as input to sequential logic circuit 1104. As a result, sequential logic circuit 1104 may sequentially perform subdivision processing for as many as four (4) subtiles which are subsequently provided as input to sequential logic circuit 1106...At this point, information related to the subtiles is sequentially provided as input to parallel logic circuit 1116. Parallel logic circuit 1116 has twice as much identical hardware than each sequential logic circuits 1102 through 1114..one output of parallel logic circuit 1116 is supplied as an input to parallel logic circuit 1118...".

A different polygonal portion refers to **a** tile or **a** subtile, according to applicant's specification.

The input to sequential logic circuit 1102 is the basic tile and the input to the sequential logic circuit 1104 is the two subtiles, etc. Thus, the logic circuit 1104 receives two subtiles of the raster image covering the same tile of the raster image as that received by the preceding logic circuit 1102. The parallel logic circuit 1116 receives the polygonal portion for the same tile of the raster image (covering up to 128 subtiles for the said tile) as that received by the sequential logic circuit 1102.

Thus, if applicant's claim limitation "a different polygonal portion" refers to a tile, each of the sequential logic circuits and each of the parallel logic circuits configured to receive the same basic tile of the raster image, in accordance to the applicant's specification, which is in contrary to what has been claimed.

Moreover, applicant's claim limitation "a different polygonal portion" cannot be a subtile. This is because each of the sequential or parallel logic circuits receives one basic tile or two or more subtiles.

In both situations analyzed in above, the specification does not describe "each of the sequential logic circuits and each of the parallel logic circuits configured to receive a different polygonal portion of the raster image."

The base claim 22 recites "wherein a maximum number of subtiles processed per cycle is a constant in each cycle of a first plurality of the number of cycles and increases for cycles of a second plurality of the number of cycles."

However, the cycle is only described in Paragraph 0072 of applicant's specification. It is stated that instead of requiring as many as 1024 cycles to determine whether all 1024 pixels in a 32 by 32 tile are inside a primitive, if such evaluations are carried out sequentially, the combination pipeline structure of Fig. 11 allows such evaluations to be made in approximately 138 cycles or less. This is because subdivisions are carried out in parallel. The specification, however, only describes a total number of cycles required to determine whether pixels in a tile are inside or outside a primitive. The specification does not describe the claim limitation "wherein a maximum number of subtiles processed per cycle is a constant in each cycle of a first plurality of the number of cycles and increases for cycles of a second plurality of the number of cycles."

There is no disclosure in applicant's specification as to "a maximum number of subtiles processed per cycle". For example, whether the Parallel Logic 1118 and the Parallel Logic 1120 requires one cycle or two cycles to process the subdivision is unknown from the specification. If one cycle is required to process the subdivision for both the Parallel Logic 1118 and the Parallel Logic 1120, the number of subtiles processed in the next cycle for the Parallel Logic 1122-1128

are different from the previous cycle. Therefore, the number of subtiles per cycle is not a constant as claimed for each cycle of a first plurality of the number of cycles. Applicant's claim limitation is not justified by the specification, in particular, Paragraph 0072 and Fig. 11.

An applicant must convey with reasonable clarity to those skilled in the art that, as of the filling date sought, he or she was in possession of the invention. Vas-Cath, Inc. v. Mahurkar, 935 F.2d 1555, 1563-64, 19 USPQ2d 1111, 1117 (Fed. Cir. 1991). For purposes of written description, one shows "possession" by descriptive means such as words, structures, figures, diagrams, and formulas that fully set forth the claimed invention. Lockwood v. American Airlines, Inc., 107 F.3d 1565, 1572, 41 USPQ2d 1961, 1966 (Fed. Cir. 1997). Such descriptive means cannot be found in the disclosure for the inventions of the base claim 22.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claims 1, and 3-11 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

The base claim 1 set forth the claim limitation "each of the sequential logic circuits and each of the parallel logic circuits configured to receive a *different polygonal portion* of the raster image".

In applicant's disclosure related to this claim limitation in Fig. 11 and the corresponding specification, for example, Page 23-24, "sequential logic circuit 1102 may sequentially perform subdivision processing and edge function... provided as input to sequential logic circuit 1104. As a result, sequential logic circuit 1104 may sequentially perform subdivision processing for as many as four (4) subtiles which are subsequently provided as input to sequential logic circuit 1106...At this point, information related to the subtiles is sequentially provided as input to parallel logic circuit 1116. Parallel logic circuit 1116 has twice as much identical hardware than each sequential logic circuits 1102 through 1114..one output of parallel logic circuit 1116 is supplied as an input to parallel logic circuit 1118...".

A different polygonal portion refers to a tile or a subtile, according to applicant's specification.

The input to sequential logic circuit 1102 is the basic tile and the input to the sequential logic circuit 1104 is the two subtiles, etc. Thus, the logic circuit 1104 receives two subtiles of the raster image covering the same tile of the raster image as that received by the preceding logic circuit 1102. The parallel logic circuit 1116 receives the polygonal portion for the same tile of the raster image (covering up to 128 subtiles for the said tile) as that received by the sequential logic circuit 1102.

Thus, if applicant's claim limitation "a different polygonal portion" refers to a tile, each of the sequential logic circuits and each of the parallel logic circuits configured to receive the

same basic tile of the raster image, in accordance to the applicant's specification, which is in contrary to what has been claimed.

Moreover, applicant's claim limitation "a different polygonal portion" cannot be a subtile. This is because each of the sequential or parallel logic circuits receives one basic tile or two or more subtiles.

In both situations analyzed in above, the specification does not describe "each of the sequential logic circuits and each of the parallel logic circuits configured to receive a different polygonal portion of the raster image."

An applicant must convey with reasonable clarity to those skilled in the art that, as of the filling date sought, he or she was in possession of the invention. Vas-Cath, Inc. v. Mahurkar, 935 F.2d 1555, 1563-64, 19 USPQ2d 1111, 1117 (Fed. Cir. 1991). For purposes of written description, one shows "possession" by descriptive means such as words, structures, figures, diagrams, and formulas that fully set forth the claimed invention. Lockwood v. American Airlines, Inc., 107 F.3d 1565, 1572, 41 USPQ2d 1961, 1966 (Fed. Cir. 1997). Such descriptive means cannot be found in the disclosure for the inventions of the base claim 1.

The claims 3-11 depend upon the base claim 1 and are rejected due to their dependency on the claim 1.

Claims 22, 24-25 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant

art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

The base claim 22 recites "wherein a maximum number of subtiles processed per cycle is a constant in each cycle of a first plurality of the number of cycles and increases for cycles of a second plurality of the number of cycles."

However, the cycle is only described in Paragraph 0072 of applicant's specification. It is stated that instead of requiring as many as 1024 cycles to determine whether all 1024 pixels in a 32 by 32 tile are inside a primitive, if such evaluations are carried out sequentially, the combination pipeline structure of Fig. 11 allows such evaluations to be made in approximately 138 cycles or less. This is because subdivisions are carried out in parallel. The specification, however, only describes a total number of cycles required to determine whether pixels in a tile are inside or outside a primitive. The specification does not describe how many cycles are required for each parallel logic circuit or each sequential logic circuit. The specification does not describe the claim limitation "wherein a maximum number of subtiles processed per cycle is a constant in each cycle of a first plurality of the number of cycles and increases for cycles of a second plurality of the number of cycles."

There is no disclosure in applicant's specification as to "a maximum number of subtiles processed per cycle". For example, whether the Parallel Logic 1118 and the Parallel Logic 1120 requires one cycle or two cycles to process the subdivision is unknown from the specification. If one cycle is required to process the subdivision for both the Parallel Logic 1118 and the Parallel Logic 1120, the number of subtiles processed in the next cycle for the Parallel Logic 1122-1128 are different from the previous cycle. Therefore, the number of subtiles per cycle is not a

constant as claimed for each cycle of a first plurality of the number of cycles. Applicant's claim limitation is not justified by the specification, in particular, Paragraph 0072 and Fig. 11.

An applicant must convey with reasonable clarity to those skilled in the art that, as of the filling date sought, he or she was in possession of the invention. Vas-Cath, Inc. v. Mahurkar, 935 F.2d 1555, 1563-64, 19 USPQ2d 1111, 1117 (Fed. Cir. 1991). For purposes of written description, one shows "possession" by descriptive means such as words, structures, figures, diagrams, and formulas that fully set forth the claimed invention. Lockwood v. American Airlines, Inc., 107 F.3d 1565, 1572, 41 USPQ2d 1961, 1966 (Fed. Cir. 1997). Such descriptive means cannot be found in the disclosure for the inventions of the base claim 22.

The claims 24-25 depend upon the claim 22 and are rejected due to their dependency on the claim 22.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1 and 3-11 rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

The base claim 1 failed to particularly point out "a *different polygonal portion*" which renders the claim 1 indefinite.

A different polygonal portion refers to a tile or a subtile.

However, if applicant's claim limitation "a different polygonal portion" refers to a tile, each of the sequential logic circuits and each of the parallel logic circuits configured to receive the same basic tile of the raster image, in accordance to the applicant's specification, which is in contrary to what has been claimed.

Applicant's claim limitation "a different polygonal portion" cannot be a subtile. This is because each of the sequential/parallel logic circuits receives a tile or more than one subtiles, precluding the assumption that a different polygonal portion being a subtile.

In both situations analyzed in above, applicant failed to particularly point out the claim limitation "each of the sequential logic circuits and each of the parallel logic circuits configured to receive a different polygonal portion of the raster image."

The claims 3-11 depend upon the base claim 1 and are rejected due to their dependency on the claim 1.

Claims 22 and 24-25 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

The base claim 22 failed to particularly point out, "a first plurality of the number of cycles" and " a second plurality of the number of cycles" as related to a maximum number of subtiles processed per cycle. This is because whether each sequential logic circuit and/or each parallel logic circuit requires one clock cycle or two clock cycles cannot be determined and

therefore there is uncertainty as to a maximum number of subtiles processed per cycle for a sequential logic circuit or a parallel logic circuit or a plurality of parallel logic circuits per cycle.

The claims 24-25 depend upon the claim 22 and are rejected due to their dependency on the claim 22.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

1. Claims 1, 4, 6-7 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Duluk et al. U.S. Pat. No. RE38,078 (hereinafter Duluk) in view of Bowen et al. U.S. Patent No. 6,329,996 (hereinafter Bowen).

2. Claim 1:

(a) Duluk teaches a system for identifying pixels inside a graphics primitive of a raster image, the system comprising:

A memory for storing a raster image (e.g., the addressable MCCAM memory structure of Figs. 33-34, and 37-38 of Duluk);

A graphics engine coupled to the memory and comprising a pipeline structure configured for both sequential and parallel processing (*e.g., Sequential processing includes the processing by*

the logic circuits with the Screen Space Conversion 1003 of the SOT 3D graphics Pipeline 31000 wherein a dual occulting test 3D graphics pipeline is disclosed; see column 46, lines 5-20 and the pixel drawing pipeline 5000, 28000 and 31000 is split into a multiplicity of smaller independent blocks; see column 38, lines 35-40; moreover, Duluk discloses in Figs. 37-38 a plurality of sequential logic circuits such as Block Convert 37004 and Edge Walk Processor 33004 sequentially connected and processing a different interleaved block each clock cycle because the interleaved block changes as clock cycle changes), the pipeline structure comprising a first plurality of sequential logic circuits in series (*Block Convert 37004 translates input data on the Translated/Geometry 2004 bus from screen coordinates to coordinates relative to the corresponding block; see column 39, lines 25-35; the screen space conversion 1003; see column 18, lines 55-65 outputs TranslateGeometry 2004 to the MCCAM pixel drawing subsystem 6002 and to the Block Convert 37004 (and Edge Walk Processor 3300) and therefore, the screen space conversion 1003, the Block Convert 37004 and Edge Walk Processor 33004 within the Block Pixel Drawing subsystem 37002 of Figs. 37-38 are sequentially connected and processing a different interleaved block per clock cycle because the interleaved block changes as clock cycle changes; column 39, lines 10-45; input to the screen space conversion 1003 is a mesh and the input to the Block Convert 37004 is a block within a mesh; bounding box information is input to the screen space conversion 1003; see column 20, lines 55-67 and MCCAM Z-buffer sequentially getting each root object from the geometry database*) and a second plurality of parallel logic circuits (*e.g., parallel logic circuits are disclosed in Duluk Figs. 37-38 the plurality of MCCAM Z-buffer in parallel performing Occulting Tests; see column 18, lines 59-62*) coupled to the first plurality of sequential logic circuits, each of the logic circuits configured to determine whether a

polygonal portion of the raster image is at least partly inside the graphics primitive (*e.g., column 37, lines 40-67 wherein the Block Convert 37004 Edge Walk Processor 33004 perform vertex bounding box occulting text in each clock cycle is performed; see column 26*).

(b) Although Duluk discloses a first plurality of sequential logic circuits in series and a second plurality of parallel logic circuits coupled to the first plurality of sequential logic circuits, each of the logic circuits configured to determine whether a polygonal portion of the raster image is at least partly inside the graphics primitive, Duluk is silent to "each of the sequential logic circuits and each of the parallel logic circuits configured to receive a different polygonal portion of the raster image".

(c) Bowen has taught a graphics pipeline structure comprising a first plurality of sequential logic circuits coupled in series and a second plurality of parallel logic circuits coupled to the first plurality of sequential logic circuits, each of the sequential logic circuits and each of the parallel logic circuits configured to receive a different polygonal portion of the raster image", (e.g., Fig. 1-3, column 3, line 60 to column 6, line 22).

(d) It would have been obvious to one of ordinary skill in the art to have combined the pipeline structure having the multiple sequential and parallel logic circuits of Bowen with Duluk in such a manner that each individual pipeline Bowen would have been the same as the pipeline of Duluk so that the combined pipeline structure as presented in Bowen's Figs. 1 and 3 would have so produced to determine whether the received polygonal portion is at least partly inside the graphics primitive because Duluk's pipeline is configured to determine whether the received polygonal portion is least partly inside the graphics primitive (Duluk *Figures 32-38; column 37).*

Moreover, the combined pipeline structure would be the same as what has been claimed, i.e., the combined pipeline structure of Bowen and Duluk comprises a first plurality of sequential logic circuits coupled in series and a second plurality of parallel logic circuits coupled to the first plurality of sequential logic circuits (Bowen Fig. 1-3, column 3, line 60 to column 6, line 22 and Duluk *Figures 32-38; column 37),* each of the sequential logic circuits and each of the parallel logic circuits configured to receive a different polygonal portion of the raster image (Bowen Fig. 1-3, column 3, line 60 to column 6, line 22) and to determine whether the received polygonal portion is at least partly inside the graphics primitive (Duluk *Figures 32-38; column 37).*

(e) One of the ordinary skill in the art would be motivated to have used a different pipeline structure having the multiple sequential and parallel logic circuits for improving the speed of the rendering process using multiple graphics pipeline (Bowen column 1, lines 40-48).

Claim 4:

The claim 4 encompasses the same scope of invention as that of claim 1 except additional claimed limitation of the pipeline structure determining whether the polygonal portion of the raster image is at least partly inside the graphics primitive by evaluating edge function of the graphics primitive on at least one corner vertex of the polygonal portion. However, Duluk further discloses the claimed limitation of the pipeline structure determining whether the polygonal portion of the raster image is at least partly inside the graphics primitive by evaluating edge function of the graphics primitive on at least one corner vertex of the polygonal portion (e.g. Duluk column 37, lines 40-67).

Claim 6:

The claim 6 encompasses the same scope of invention as that of claim 4 except additional claimed limitation of the edge functions being evaluated on at least one corner vertex of the polygonal portion, to determine a corner vertex of the polygonal portion being from a primitive edge associated with the edge function in a direction toward the inside of the graphics primitive. However, Duluk further discloses the claimed limitation of the edge functions being evaluated on at least one corner vertex of the polygonal portion, to determine a corner vertex of the polygonal portion being from a primitive edge associated with the edge function in a direction toward the inside of the graphics primitive (e.g., Duluk column 22, lines 1-43; column 32, lines 55-62; column 37, lines 40-67, column 38, lines 41 through column 39, line 43).

Claim 7:

The claim 7 encompasses the same scope of invention as that of claim 1 except additional claimed limitation of the sequential logic circuits followed by the parallel logic circuits. However, Duluk further discloses the claimed limitation of the sequential logic circuits followed by the parallel logic circuits (e.g., Duluk Figure 38).

Claim 10:

The claim 10 encompasses the same scope of invention as that of claim 1 except additional claimed limitation of the pipeline structure further comprising a predetermined number

of pixel engines coupled to at least some of the parallel logic circuits and configured to determine attribute values associated with each pixel. However, Duluk further discloses the claimed limitation of the pipeline structure further comprising a predetermined number of pixel engines coupled to at least some of the parallel logic circuits and configured to determine attribute values associated with each pixel (e.g., Duluk Fig. 38).

3. Claim 5 is rejected under 35 U.S.C. 103(a) as being as being unpatentable over Duluk et al. U.S. Pat. No. 6,664,959 (hereinafter Duluk) and Bowen et al. U.S. Patent No. 6,329,996 (hereinafter Bowen), in view of Greene et al. U.S. Patent No. 6,480,205 (hereafter Greene).

Claim 5:

(1) The claim 5 encompasses the same scope of invention as that of claim 4 except additional claimed limitation of each edge function of the graphics primitive being the vector function comprising both an x-component and a y-component of a vector normal to the edge function.

(2) However, Duluk and Bowen are silent to the claim limitation of each edge function of the graphics primitive being the vector function comprising both an x-component and a y-component of a vector normal to the edge function.

(3) Greene discloses the claimed limitation of each edge function of the graphics primitive being the vector function comprising both an x-component and a y-component of a vector normal to the edge function (Greene column 18).

(4) It would have been obvious to one of ordinary skill in the art to have incorporated the Greene's edge function and normal vectors into Duluk and Bowen's method for determining whether the corners of the regions are within, outside, or fully inside a graphical primitive because Duluk suggests determining whether a tile within a graphics primitive (Duluk column 37) which involves calculating the left most and right most positions of the primitive in each subraster line that contains at least one sample point and therefore suggesting an obvious modification of Duluk and Bowen.

(5) One having the ordinary skill in the art would have been motivated to do this because it would have provided an edge equation for determining whether a portion of tile is covered by a graphics primitive (*e.g., determining the corner of the cell wherein the plane of the polygon is nearest using the quadrant vector being normal to the polygon; see Greene column 18*).

4. Claims 8 is rejected under 35 U.S.C. 103(a) as being as being unpatentable over Duluk et al. U.S. Pat. No. 6,664,959 (hereinafter Duluk) and Bowen et al. U.S. Patent No. 6,329,996 (hereinafter Bowen), in view of Greene U.S. Patent No. 6,480,205 (hereinafter Greene).

Claim 8:

(1) The claim 8 encompasses the same scope of invention as that of claim 1 except additional claimed limitation of parallel logic circuits coupled together in a pyramid structure.

(2) However, Duluk and Bowen are silent to the claim limitation of parallel logic circuits coupled together in a pyramid structure.

(3) Greene teaches a pyramid structure for processing a tile before processing other cells in the tile in hierarchical polygon tiling (Greene column 15-17).

(4) It would have been obvious to one of ordinary skill in the art to have incorporated Greene's pyramid structure for tiling into the Duluk and Bowen's system because Duluk's State Machines are arranged in parallel and can be arranged to process the tile stack such as the pyramid of tiles (Duluk Fig. 38) and therefore suggesting an obvious modification of Duluk and Bowen.

(5) One having the ordinary skill in the art would have been motivated to do this because it would have changed the parallel logic circuits in a pyramid structure to corresponds to the pyramid tile stacks and to determine any visible samples on the polygon (Greene column 16).

5. Claim 3, 9 and 11 is rejected under 35 U.S.C. 103(a) as being as being unpatentable over Duluk et al. U.S. Pat. No. 6,664,959 (hereinafter Duluk) and Bowen et al. U.S. Patent No. 6,329,996 (hereinafter Bowen), in view of Larson U.S. Pat. No. 6,359,623 (hereinafter Larson).

Re Claims 3 and 9:

The claim 3 (9) encompasses the same scope of invention as that of claim 1 except additional claim limitation of the pipeline structure configured to divide the polygonal portion into a predetermined number of polygonal subportions if the polygonal porition is at least partly inside the graphics primitive.

Duluk and Bowen are silent to the claim limitation of the pipeline structure configured to divide the polygonal portion into a predetermined number of polygonal subportions if the polygonal porition is at least partly inside the graphics primitive.

Larson teaches a method for identifying pixels inside a graphics primitive of a raster image (see the abstract, figures 6-10) comprising the steps of:

Selecting a tile including a pixel (column 10, lines 42-54);

Determining if a portion of the tile is within the graphics primitive (column 10, lines 55-67, column 11, lines 1-16);

Dividing the tile into sub-tiles if a portion of the tile is within the graphics primitive and another portion of the tile is outside the graphics primitive (column 11, lines 1-16);

Recursively dividing each sub-tile larger than a pixel having a portion within the graphics primitive and another portion outside the graphics primitive into subtiles (figure 4, column 11, lines 1-16).

It would have been obvious to one of ordinary skill in the art to have incorporated Larson's division into the polygonal subportions if the polygonal portion being at least partly inside the graphics primitive into the Duluk and Bowen's system because Duluk suggests sub-dividing the tiles and coordinate transformation (Duluk column 38, lines 26-40) and therefore suggesting an obvious modification of Duluk and Bowen.

One having the ordinary skill in the art would have been motivated to do this because it would have provided a subdivision of a tile based on edge equation (Larson column 30).

However, Duluk, Bowen and Larson is silent to subdividing the polygonal portion into two polygonal subportions.

It would have been obvious to one of ordinary skill in the art to have subdivided the basic tile into two subtiles because Larson teaching dividing the tile into a number of subtiles wherein the number includes two.

One of the ordinary skill in the art would have been motivated to dividing a tile into just two subtiles to perform the occulusion test (See Larson column 11, lines 1-16).

Re Claim 11:

(1) The claim 11 encompasses the same scope of invention as that of claim 1 except additional claimed limitation of the polygonal portion of a raster image having a width and a height, each of the width and the height having a value of a power of 2^m.

(2) Duluk and Bowen are silent to the claim limitation of the polygonal portion of a raster image having a width and a height, each of the width and the height having a value of a power of 2^m.

(3) Larson discloses the claimed limitation of the polygonal portion of a raster image having a width and a height, each of the width and the height having a value of a power of 2^m (e.g., 16 by 16 subpixels; see column 30).

(4) It would have been obvious to one of ordinary skill in the art to have incorporated Larson's specific selection of width and height for the polygonal portions into the Duluk and Bowen's system because Duluk suggests sub-dividing the tiles and coordinate transformation (Duluk column 38, lines 26-40) and therefore suggesting an obvious modification of Duluk and Bowen.

(5) One having the ordinary skill in the art would have been motivated to do this because it would have provided a bit wise operation for coordinate transformation (Larson column 30).

6. Claims 22, 24-25 are rejected under 35 U.S.C. 103(a) as being as being unpatentable over Larson U.S. Pat. No. 6,359,623 (hereinafter Larson), in view of Greene et al. U.S. Patent No. 6,480,205 (hereafter Greene).

7. Claim 22:

(1) Larson teaches a method for identifying pixels inside a graphics primitive of a raster image (see the abstract, figures 6-10) comprising the steps of:

Selecting a tile including a pixel (column 10, lines 42-54);

Determining if a portion of the tile is within the graphics primitive (column 10, lines 55-67, column 11, lines 1-16);

Dividing the tile into sub-tiles if a portion of the tile is within the graphics primitive and another portion of the tile is outside the graphics primitive (column 11, lines 1-16);

Recursively dividing each sub-tile larger than a pixel having a portion within the graphics primitive and another portion outside the graphics primitive into subtiles (figure 4, column 11, lines 1-16).

However, Larson does not implicitly disclose dividing the tile into two subtiles as claimed, although Larson explicitly teach dividing the tile into a number of subtiles.

It would have been obvious to one of ordinary skill in the art to have subdivided the basic tile into two subtiles because Larson teaching dividing the tile into a number of subtiles wherein the number includes two.

One of the ordinary skill in the art would have been motivated to dividing a tile into just two subtiles to perform the occulusion test (See Larson column 11, lines 1-16).

However, it remains to show that Larson and Greene teaches or suggests the claim limitation "wherein a maximum number of subtiles processed per cycle is a constant in each cycle of a first plurality of the number of cycles and increases for cycles of a second plurality of the number of cycles."

Greene teaches a subdivision of the preceding subtile or tile. As tiles are sub-divided into sub-tiles and sub-tiles are further divided into smaller sub-tiles, the number of subtiles processed per cycle change with respect to the number of clock cycle of the plurality of clock cycles. Greene therefore teaches the claim limitation "wherein a maximum number of subtiles processed per cycle is a constant in each cycle of a first plurality of the number of cycles and increases for cycles of a second plurality of the number of cycles."

It is also noted that Greene teaches the number of subtiles processed vary with respect to the coordinate reference frame location and subdivision process and therefore subtiles processed per cycle may vary with respect to the subdivision process.

It would have been obvious to one of ordinary skill in the art to have incorporated the Greene's subdivision of tiles into sub-tiles for determining whether the corners of the regions are within, outside, or fully inside a graphical primitive.

One having the ordinary skill in the art would have been motivated to do this because it would have divided a basic tile into a number subtiles that permits the equations to be evaluated with shifts and adds (Greene column 21, lines 59-67; column 22, lines 1-45).

Claim 24:

The claim 24 encompasses the same scope of invention as that of claim 22 except additional claimed limitation that the step of determining further comprises evaluating the tile at a corner vertex which is farthest in a direction toward the inside of the graphics primitive relative to an edge of the graphics primitive. However, Larson and Greene further disclose the claimed limitation that the step of determining further comprises evaluating the tile at a corner vertex which is farthest in a direction toward the inside of the graphics primitive relative to an edge of the graphics primitive (Larson column 10, lines 55-67; Greene column 18).

Claim 25:

The claim 25 encompasses the same scope of invention as that of claim 22 except additional claimed limitation that the step of recursively dividing further comprises determining if the sub-tile is at least partly within the graphics primitive by evaluating the sub-tile at a corner vertex which is farthest in a direction toward the inside of the graphics primitive relative to an edge of the graphics primitive. However, Larson and Greene further disclose the claimed limitation that the step of recursively dividing further comprises determining if the sub-tile is at least partly within the graphics primitive by evaluating the sub-tile at a corner vertex which is farthest in a direction toward the inside of the graphics primitive relative to an edge of the graphics primitive (Larson column 10, lines 55-67; Greene column 18).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jin-Cheng Wang whose telephone number is (571) 272-7665. The examiner can normally be reached on 8:00 - 6:30 (Mon-Thu).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kee Tung can be reached on (571) 272-7794. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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jcw Jincheng Wang